UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,620	10/16/2001	Richard L. Coulson	5038-118	6345

8791 7590 04/01/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
VERBRUGGE, KEVIN	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,620	COULSON, RICHARD L.	
	Examiner	Art Unit	
	Kevin Verbrugge	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37 and 40-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37 and 40-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This non-final Office action is in response to the affidavit filed 10/20/04 by fax which was submitted in an attempt to disqualify the Nordal reference. The affidavit is persuasive, therefore the rejection based on the Nordal reference is withdrawn. Claims 1-37 and 40-84 remain pending. The claims are newly rejected based on a new reference as cited below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-37 and 40-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,860,083 to Sukegawa in view of the IBM Technical Disclosure Bulletin NN9411421 published 11/1/94, hereinafter simply the TDB.

Regarding claims 1, 2, 8, 9, 15, 16, 17, 19, 20, 21, 26, 27, 28, 29, 30, 31, 34, 35, 36, 37, 73, 74, 75, 80, 81, 82, 83, and 84, Sukegawa shows the claimed hard disk as hard disk drive (HDD) 2 in Fig. 1. He shows the claimed cache memory as non-volatile

cache area 10C inside flash memory unit 1. He shows the claimed memory controller as cache system controller 3.

Sukegawa's memory controller determines if a memory request can be satisfied by accessing the cache memory as claimed. If it can be satisfied by the cache (such as when a read request or a write request hits the cache), then it is satisfied by the cache (see Sukegawa column 7, 30-39). If it cannot be satisfied by the cache (such as when a write misses the cache), then it is queued up and executed when the hard disk drive is accessed as claimed (see Sukegawa column 10, lines 5-17).

Sukegawa does not teach that his non-volatile memory is a polymer ferroelectric memory, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to make it so for the attendant advantages of polymer ferroelectric memory.

The TDB teaches that it was known to use polymer ferroelectric memories for nonvolatile storage purposes. As taught by the TDB, polymer ferroelectric memory was a known type of nonvolatile memory at the time of the invention and it therefore would have been an obvious choice to use for the nonvolatile memory in Sukegawa's device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a polymer ferroelectric memory for the design benefits that it provides, including small size, inexpensive construction, and fast response times.

Regarding claim 3, Sukegawa's memory controller processes digital signals and is therefore a digital signal processor. If Applicants dispute this interpretation of DSP,

then specific reference must be made to the specification to show why this interpretation of DSP is inappropriate.

Regarding claim 4, Sukegawa's memory controller is an integrated circuit with a specific application (controlling memory) and is therefore an ASIC. If Applicants dispute this interpretation of ASIC, then specific reference must be made to the specification to show why this interpretation of ASIC is inappropriate.

Regarding claims 5, 32, and 33, Sukegawa does not teach that his cache system controller comprises software running on a host processor. However, he shows a host processor as host system 4 in Fig. 1 and it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the cache system controller in software to make it more flexible, upgradeable, etc.

Regarding claim 6, Sukegawa 's memory controller resides with the cache in the apparatus of Fig. 1.

Regarding claim 7, Sukegawa's memory controller is shown separate from the cache and the hard disk as claimed.

Regarding claims 10, 11, 22, and 23, Sukegawa teaches that queuing up memory writes reduces the frequency of access to his disk drive thereby saving power

at column 10, lines 5-17. Furthermore, at column 7, lines 8-12 he explicitly teaches that the BIOS can start the system without activating the disk drive, thereby saving power. From these two passages, it is clear that in some situations, accessing Sukegawa's hard disk comprises spinning up the hard disk first, as claimed.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to spin down the hard disk whenever activity was low to save power. The question of when to spin it down is a design choice taking into account power savings vs. performance degradation. In any case, once the disk is spun down, further accesses to the disk require it to be spun up first, as claimed.

Regarding claims 14, 18, and 53, Sukegawa does not teach determining if queued operations are desirable and then performing only the operations that are desirable. However, Official Notice is taken of queue operation techniques whereby more recent queue entries make older queue entries obsolete and therefore undesirable. Those undesirable queue entries are then deleted to avoid wasted operations. This typically includes memory requests to the same address where a first write to a certain address is made obsolete by a later write to the same address, for example. Since the first write is still in the queue (and has therefore not been written to memory) when the second write to the same address is placed in the queue, the first write can be deleted with no consequence to program operation as long as there are no intervening reads to that same address.

Regarding claims 40, 41, 42, 43, 45, 46, 47, 48, 49, 50, 51, 52, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 67, 68, 72, 76, 77, 78, and 79, Sukegawa's device clearly can begin operation without spinning up the hard disk as discussed in the rejection of claim 10. His BIOS reads the necessary data from the flash memory to boot up the machine and get the operating system and one or more application programs up and running. Furthermore, he clearly teaches queuing first access requests (new data writes) as discussed in the rejection of claim 1.

What he doesn't say but what is readily apparent is that once certain access requests (such as reads) are received that cannot be satisfied from the flash memory, the hard disk must be spun up to satisfy the requests. What is obvious is that once the disk is then spun up, the queued requests can quickly and efficiently be "unqueued" or sent to the disk, completing them as claimed.

Regarding claims 12, 13, 24, 25, 44, 66, and 69, Sukegawa does not mention prefetches, but Official Notice is taken that prefetching was well-known in the art at the time of the invention. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement prefetching in Sukegawa's device to improve system operation by fetching data before it was needed to reduce operation time (the known benefit of prefetching).

One of the more effective uses of prefetching is for sequential streams. Once a processor determines that a request is part of a sequential stream, prefetching is implemented to obtain subsequent data of the sequential stream before it is actually

needed so that when it is actually needed, it already resides in the cache and can be accessed quickly from the cache. If a request is not part of a sequential stream, prefetching may or may not be useful (overly aggressive prefetching results in storing data in the cache that will never be used, forcing data in the cache that would have been used again to be thrown out). Prefetching is always a design tradeoff between gaining the speed advantage of having prefetched data in the cache before it is actually requested and throwing out data that will be used again to make room for prefetched data that might not be used. The small size of a cache is what makes prefetching potentially more detrimental than beneficial to operating speed.

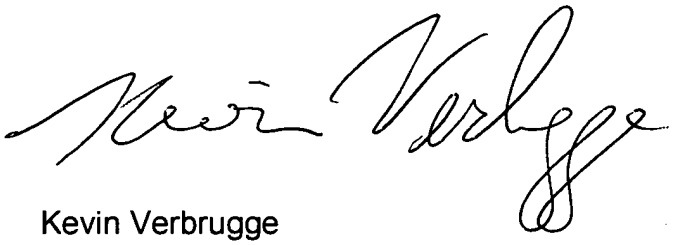
Regarding claims 70 and 71, Sukegawa does not disclose that his device caches data associated with a multimedia sequential stream, however, his device can be used with all kinds of data, including multimedia sequential streams.

Conclusion

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (571) 272-4214.

Any response to this action should be labeled appropriately (including serial number, Art Unit 2189, and type of response) and mailed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, hand-carried or delivered to the Customer Service Window at Randolph Building, 401 Dulany Street, Alexandria, VA 22313, or faxed to (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.



Kevin Verbrugge
Primary Examiner
Art Unit 2189